CLAIMS

What is claimed is:

1. An apparatus for inserting one or more data bytes into a stream of data words, comprising:

a first circuit to generate a first and a second intermediate data word correspondingly containing first and second zero or more data bytes of a first data word of a preceding cycle, said first and second zero or more data bytes being data bytes that precede and follow a first data byte insertion point of the preceding cycle respectively, and said first and second zero or more data bytes being repositioned within said first and second intermediate data words respectively, with said first zero or more data bytes being repositioned within said first intermediate data word relative to cascaded alignment impact of cycles prior to said preceding cycle, and said second zero or more data bytes being repositioned within said second intermediate data word relative to said cascaded alignment impact of cycles prior to said preceding cycle, said first data byte insertion point of the preceding cycle, and a first number of data bytes inserted after said first data byte insertion point of the preceding cycle;

a second circuit to generate a first re-aligned variant of a first insertion data word containing said first number of data bytes inserted during said preceding cycle; and

a third circuit coupled to said first and second circuits to generate an output data word conditionally using selected parts of said first and second intermediate data words, and said first re-aligned variant of the first insertion data word.

2. The apparatus of claim 1, wherein said first circuit comprises an arithmetic operator, a first and a second logic operator, a first selector coupled to said first logic operator, and a second selector coupled to said arithmetic operator and said second logic operator to generate a first position pointer pointing to a first data byte position after which said data byte insertion of the preceding cycle began, and a second position pointer pointing to a second data byte position at which said data byte insertion of the preceding cycle ended, respectively.

3. The apparatus of claim 1, wherein

said apparatus further comprises a register to a store a shift amount for shifting said first data word of the preceding cycle to generate said first intermediate data word with said first zero or more data bytes before said first data byte insertion point of the preceding cycle repositioned relative to cascaded alignment impact of cycles prior to said preceding cycle; and

said first circuit comprises an arithmetic operator and a selector coupled to the arithmetic operator to generate a second shift amount for shifting said first data word of the preceding cycle to generate said second intermediate data word with said second zero or more data bytes after said first data byte insertion point of the preceding cycle repositioned relative to said cascaded alignment impact of cycles prior said preceding cycle, said first data byte insertion point of the preceding cycle, and said first number of data bytes inserted after said first data byte insertion point of the preceding cycle.

4. The apparatus of claim 1, wherein said first circuit further comprises a bit concatenator, a plurality of arithmetic operators, and a plurality of shifters correspondingly coupled to the concatenator and the arithmetic operators to

generate said first and second intermediate data words with said first and second zero or more data bytes repositioned accordingly.

5. The apparatus of claim 1, wherein said second circuit comprises a concatenator and a shifter coupled to the concatenator to generate said re-aligned variant of said first insertion data word containing said first number of data bytes inserted.

6. The apparatus of claim 1, wherein said third circuit comprises data bit selection logic that conditionally selects data bits from said first and second intermediate data words and said first re-aligned variant of the first insertion data word to form said output data word.

7. The apparatus of claim 6, wherein said selection logic conditionally selects data bits from said first and second intermediate data words and said first re-aligned variant of the first insertion data word to form said output data word, in accordance with a plurality of multi-bit data bit selection masks.

8. The apparatus of claim 7, wherein said selection logic conditionally selects a data bit from said first intermediate data word if the corresponding data bits of said data bit selection masks form a "110" data bit pattern, from said second intermediate data word if the corresponding data bits of said data bit selection masks form a "101" data bit pattern, and from said first re-aligned variant of the first insertion data word if the corresponding data bits of said data bit selection masks form a "100" data bit pattern.

9. The apparatus of claim 1, wherein said apparatus further comprises one or more registers for storing at least a selected one of said first data word, a first shift amount said first data word was shifted to accommodate cascaded alignment impact of cycles prior to said preceding cycle, a second shift amount said first data word was shifted to accommodate cascaded alignment impact of cycles prior to said preceding cycle and said first number of data bytes inserted after said first data byte insertion point of the preceding cycle, a first data byte position after which said first number of data bytes of the preceding cycle was inserted, a second data byte position at which insertion of said first number of data bytes of the preceding cycle ended, and an overflow indicator indicating an insertion overflow condition.

10. The apparatus of claim 1, wherein the apparatus further comprises fourth circuitry to generate a plurality of multi-bit data bit selection masks for use by said third circuitry in forming said output data word, conditionally using selected parts of said first and second intermediate data words, and said first re-aligned variant of the first insertion data word.

11. The apparatus of claim 10, wherein said fourth circuitry comprises a plurality of shifters, a first plurality of logical operators correspondingly coupled to selected ones of said shifters, and a second plurality of logical operators correspondingly coupled to selected ones of said first logical operators for generating said multi-bit data bit selection masks.

12. The apparatus of claim 1, wherein

a fourth circuit to generate a third and a fourth intermediate data word correspondingly containing third and fourth zero or more data bytes of a second data word of a current cycle, said third and fourth zero or more data bytes being data

bytes that precede and follow a second data byte insertion point of the current cycle respectively, and said third and fourth zero or more data bytes being repositioned within said third and fourth intermediate data words respectively, with said third zero or more data bytes being repositioned within said third intermediate data word relative to cascaded alignment impact of cycles prior to said current cycle, and said fourth zero or more data bytes being repositioned within said fourth intermediate data word relative to said cascaded alignment impact of cycles prior to said current cycle, said second data byte insertion point of the current cycle, and a second number of data bytes to be inserted after said data byte insertion point of the current cycle;

a fifth circuit to generate a second re-aligned variant of a second insertion data word containing said second number of data bytes of the current cycle to be inserted; and

said third circuit is also coupled to said third and fourth circuits, and conditionally uses selected parts of said third and fourth intermediate data words, and said second re-aligned variant of the second insertion data word to generate said output data word.

13. The apparatus of claim 12, wherein said fourth circuit comprises a plurality of arithmetic operators selectively coupled to each other in a pre-determined manner to generate a first position pointer pointing to a first data byte position after which said second data byte insertion of the current cycle began, and a second position pointer pointing to a second data byte position at which said second data byte insertion of the current cycle ended, respectively.

14. The apparatus of claim 12, wherein

said apparatus further comprises a register to a store a shift amount for shifting said second data word of the current cycle to generate said third intermediate data word with said third zero or more data bytes before said second data byte insertion point of the current cycle repositioned relative to cascaded alignment impact of cycles prior to said current cycle; and

said fourth circuit comprises an arithmetic operator coupled to the register to generate a second shift amount for shifting said second data word of the current cycle to generate said fourth intermediate data word with said fourth zero or more data bytes after said second data byte insertion point of the current cycle repositioned relative to said cascaded alignment impact of cycles prior to said current cycle, said second data byte insertion point of the current cycle, and said second number of data bytes inserted after said second data byte insertion point of the current cycle.

15. The apparatus of claim 12, wherein said fourth circuit further comprises a plurality of arithmetic operators and a plurality of shifters correspondingly coupled to the arithmetic operators to generate said third and fourth intermediate data words with said third and fourth zero or more data bytes repositioned accordingly.

16. The apparatus of claim 12, wherein said fifth circuit comprises a shifter to generate said re-aligned variant of said second insertion data word of the current cycle, containing said second number of data bytes of the current cycle to be inserted.

17. The apparatus of claim 12, wherein said third circuit comprises data bit selection logic that conditionally selects data bits from said third and fourth intermediate data words and said second re-aligned variant of the second insertion data word to form said output data word.

18. The apparatus of claim 17, wherein said selection logic conditionally selects data bits from said third and fourth intermediate data words and said second re-aligned variant of the second insertion data word to form said output data word, in accordance with a plurality of multi-bit data bit selection masks.

19. The apparatus of claim 18, wherein said selection logic conditionally selects a data bit from said third intermediate data word if the corresponding data bits of said data bit selection masks form a "010" data bit pattern, from said fourth intermediate data word if the corresponding data bits of said data bit selection masks form a "001" data bit pattern, and from said second re-aligned variant of the second insertion data word if the corresponding data bits of said data bit selection masks form a "000" data bit pattern.

20. The apparatus of claim 12, wherein the apparatus further comprises sixth circuitry to generate a plurality of multi-bit data bit selection masks for use by said third circuitry in forming said output data word, conditionally using selected parts of said third and fourth intermediate data words, and said second realigned variant of the second insertion data word.

21. The apparatus of claim 20, wherein said sixth circuitry comprises a plurality of shifters, a first plurality of logical operators correspondingly coupled to selected ones of said shifters, and a second plurality of logical operators correspondingly coupled

to selected ones of said first logical operators for generating said multi-bit data bit selection masks.

22. The apparatus of claim 1, wherein the apparatus is a selected one of an application specific integrated circuit, a micro-controller, a digital signal processor, a general purpose microprocessor, and a network processor.

23. An apparatus for inserting one or more data bytes into a stream of data words, comprising:

a first circuit to generate a first and a second intermediate data word correspondingly containing first and second zero or more data bytes of a first data word of a current cycle, said first and second zero or more data bytes being data bytes that precede and follow a first data byte insertion point of the current cycle respectively, and said first and second zero or more data bytes being repositioned within said first and second intermediate data words respectively, with said first zero or more data bytes being repositioned within said first intermediate data word relative to cascaded alignment impact of cycles prior to said current cycle, and said second zero or more data bytes being repositioned within said second intermediate data word relative to said cascaded alignment impact of cycles prior to said current cycle, said first data byte insertion point of the current cycle, and a first number of data bytes to be inserted after said first data byte insertion point of the current cycle;

a second circuit to generate a first re-aligned variant of a first insertion data word containing said first number of data bytes to be inserted during said current cycle; and

a third circuit coupled to said first and second circuits to generate an output data word conditionally using selected parts of said first and second intermediate data words, and said first re-aligned variant of the first insertion data word.

24. The apparatus of claim 23, wherein said first circuit comprises a plurality of arithmetic operators selectively coupled to each other in a pre-determined manner to generate a first position pointer pointing to a first data byte position after which said second data byte insertion of the current cycle began, and a second position pointer pointing to a second data byte position at which said second data byte insertion of the current cycle ended, respectively.

25. The apparatus of claim 23, wherein

said apparatus further comprises a register to a store a shift amount for shifting said first data word of the current cycle to generate said first intermediate data word with said first zero or more data bytes before said first data byte insertion point of the current cycle repositioned relative to cascaded alignment impact of cycles prior to said current cycle; and

said first circuit comprises an arithmetic operator coupled to the register to generate a second shift amount for shifting said first data word of the current cycle to generate said second intermediate data word with said second zero or more data bytes after said first data byte insertion point of the current cycle repositioned relative to said cascaded alignment impact of cycles prior to said current cycle, said first data byte insertion point of the current cycle, and said first number of data bytes inserted after said first data byte insertion point of the current cycle.

26. The apparatus of claim 23, wherein said first circuit further comprises a plurality of arithmetic operators and a plurality of shifters correspondingly coupled to the arithmetic operators to generate said first and second intermediate data words with said first and second zero or more data bytes repositioned accordingly.

27. The apparatus of claim 23, wherein said second circuit comprises a shifter to generate said re-aligned variant of said first insertion data word of the current cycle, containing said first number of data bytes of the current cycle to be inserted.

28. The apparatus of claim 23, wherein said third circuit comprises data bit selection logic that conditionally selects data bits from said first and second intermediate data words and said first re-aligned variant of the first insertion data word to form said output data word.

29. The apparatus of claim 28, wherein said selection logic conditionally selects data bits from said first and second intermediate data words and said first re-aligned variant of the first insertion data word to form said output data word, in accordance with a plurality of multi-bit data bit selection masks.

30. The apparatus of claim 29, wherein said selection logic conditionally selects a data bit from said first intermediate data word if the corresponding data bits of said data bit selection masks form a "010" data bit pattern, from said second intermediate data word if the corresponding data bits of said data bit selection masks form a "001" data bit pattern, and from said first re-aligned variant of the first insertion data word if the corresponding data bits of said data bit selection masks form a "000" data bit pattern.

31. The apparatus of claim 23, wherein the apparatus further comprises fourth circuitry to generate a plurality of multi-bit data bit selection masks for use by said third circuitry in forming said output data word, conditionally using selected parts of said first and second intermediate data words, and said first realigned variant of the first insertion data word.

32. The apparatus of claim 31, wherein said fourth circuitry comprises a plurality of shifters, a first plurality of logical operators correspondingly coupled to selected ones of said shifters, and a second plurality of logical operators correspondingly coupled to selected ones of said first logical operators for generating said multi-bit data bit selection masks.

33. The apparatus of claim 23, wherein the apparatus is a selected one of an application specific integrated circuit, a micro-controller, a digital signal processor, a general purpose microprocessor, and a network processor.

34. An apparatus for inserting one or more data bytes into a stream of data words, comprising:

a first circuit to generate a plurality of multi-bit data bit selection masks; and

a second circuit coupled to said first circuit to generate an output data word conditionally using selected parts of a first and a second intermediate data word generated from a first input data word of a current cycle, a third and a fourth intermediate data word generated from a second input data word of a preceding cycle, a first re-aligned variant of a first insertion data word of the current cycle, and a second re-aligned variant of a second insertion data word of the preceding cycle, in accordance with said data bit selection masks.

35. The apparatus of claim 34, wherein second circuit comprises selection logic that conditionally selects a data bit from said first intermediate data word if the corresponding data bits of said data bit selection masks form a "010" data bit pattern, from said second intermediate data word if the corresponding data bits of said data bit selection masks form a "001" data bit pattern, and from said first re-

aligned variant of the first insertion data word if the corresponding data bits of said data bit selection masks form a "000" data bit pattern.

36. The apparatus of claim 34, wherein said second circuit comprises selection logic that conditionally selects a data bit from said third intermediate data word if the corresponding data bits of said data bit selection masks form a "110" data bit pattern, from said fourth intermediate data word if the corresponding data bits of said data bit selection masks form a "101" data bit pattern, and from said second re-aligned variant of the second insertion data word if the corresponding data bits of said data bit selection masks form a "100" data bit pattern.

37. The apparatus of claim 34, wherein said first circuitry comprises a plurality of shifters, a first plurality of logical operators correspondingly coupled to selected ones of said shifters, and a second plurality of logical operators correspondingly coupled to selected ones of said first logical operators for generating said multi-bit data bit selection masks.

38. The apparatus of claim 34, wherein the apparatus is a selected one of an application specific integrated circuit, a micro-controller, a digital signal processor, a general purpose microprocessor, and a network processor.